REMARKS

Telephone Conference of April 8, 2005

This response is filed further to a telephone conference between Examiner Roberta Stevens and Edward Fan (Reg.No. 56,493) on April 8, 2005. In the conference, Mr. Fan indicated to Examiner that the Office Action did not appear to fully consider that the feature of beginning transmission between boundaries of time units of a transmission rate, as defined in the claims, is not described in the cited references. Examiner Stevens indicated that she would consider this aspect in greater detail. As Applicant has not received a further indication from the Examiner in this regard, Applicant provides further written submissions in this regard herebelow.

35 U.S.C. § 103

In the last Office Action of December 16, 2004, Examiner rejected claims 1, 3-10, 12, 13, 15-37, 39, 40 and 43-49 under 35 U.S.C. § 103(a) as being unpatentable over Hiltner (U.S. 5119368) in view of Pawelski (U.S. 6307869 B1). Applicant traverses the rejection as follows.

In Applicant's response to a previous Action dated October 20, 2004, Applicant amended independent claims 1, 6, 8, 10, 13, 18, 20, 22, 33, 44 and 45, to define transmission of data that begins *at a time between boundaries of time units of a transmission rate*. This feature as defined in the claims is not taught by Pawelski or Hiltner.

In the Office Action of December 16, 2005, Examiner referred to figure 3 of Hiltner in suggesting that this aspect of the claims to be described by Hiltner. However, figure 3 of Hiltner merely shows an apparatus directed to the replication of data, and this figure does not teach beginning transmission of data at a time between boundaries of time units of a transmission rate, as defined in the claims of the subject application. Applicant can find no related description in Hiltner, and in particular related to figure 3, teaching transmission of data between boundaries of time units of a transmission rate. More particularly, figure 3 of Hiltner only describes replication of data which is transmitted at a boundary of a time slot: see column 3, lines 32 to 43 of Hiltner. See also column 6, lines 37 to 39: "...an ATM cell...is read out of a FIFO buffer 403 repeatedly,...*this happens only at frame 201 boundaries*..." [emphasis addcd].

Further, Pawelski, also does not describe the invention as claimed. In fact, its system is directed to an opposite motivation: it teaches a system which provides alignment of out-of-phase input data to a reference signal (see for example, Figure 7 and column 3, lines 41 to 54). In Pawelski, the re-aligned output data is matched to the reference signal, and transmitted at the boundary of a transmission rate, such as an output clock signal (see for example, signals 28, 30 and 32 of Figure 7 of Pawelski). Pawelski does not teach beginning transmission of a traffic stream at a time between boundaries of time units, per the claims.

In view of the above, Applicant respectfully submits that independent claims 1, 6, 8, 10, 13, 18, 20, 22, 33, 44 and 45 are not obvious in view of Pawelski or Hiltner. Since all remaining claims, except for claim 50 (discussed supra), depend directly or indirectly from such independent claims, the rejection of such dependent claims is also traversed.

Furthermore, as noted in Applicant's response of October 20, 2004, Applicant submits that there is no motivation for one of ordinary skill in the art to combine Pawelski with Hiltner to arrive at Applicant's claimed invention. Again, Pawelski is directed to "recovering the phase of the *upstream data link* in a communication system" and its teachings are directed to the context of upstream data flow (see column 2, lines 7 to 10 of Pawelski, emphasis added). Hiltner, on the other hand, is directed to a broadcast or multi-cast, i.e., *downstream*, communication system (see for example, column 2, lines 23 to 25 and abstract of Hiltner). Hiltner and Pawelski are directed to different purposes of solving different problems, and as such there would be no motivation to combine such references. Additionally, independent claims 1, 10, 13, 44 and 45 of the subject application are directed to replicating data streams as data sources to *test* a multi-port communication device, as stated in the preambles of such claims. As noted above, nether Hiltner nor Pawelski is directed to test equipment or test signal generation. Thus, one of ordinary skill in the art would not arrive at a method or system for *testing* a multi-port communication device as recited in such claims, even if it were permissible to combine Hiltner and Pawelski.

For at least the above reasons, Applicant respectfully submits that the claims of the subject application, as presented on October 20, 2004, are non-obvious and patentable over the Hiltner and Pawelski, and Applicant respectfully requests that all rejections under 35 U.S.C. §103(a) be withdrawn.

Allowed Subject Matter

Examiner objected to claim 50 as being dependent from a rejected base claim, but indicated that the claim is allowable if rewritten in independent form. Applicant herein amends claim 50 to include all features of base claim 45. Claim 46 remains dependent from claim 50. Applicant submits that claims 50 and 46 are allowable.

Additional Submissions

Allowed claim 50 is directed, in part, to having a FIFO logical buffer of a given size, and at least another FIFO buffer of a different size than the given size. Applicant respectfully submits that other claims directed to buffer sizes are also allowable.

In claims 19 and 47, each claim provides a phase delay utilizing a buffer size or length, respectively, associated with a data stream and a transmission rate. In the Action of December 16, 2004, Examiner rejected such claims on the basis of figure 4 of Hiltner. While figure 4 and its associated description describe a FIFO buffer, such buffer is not used in relation of providing a phase delay. Rather, the purpose of the buffer in Hiltner is to store data from separate time slots to permit replication of such data on the output ports of the system of Hiltner. There is no teaching as to using the buffer size or length to determine phase delay in Hiltner. In this respect, Examiner has even agreed that "Hiltner does not specifically teach on traffic stream of the plurality of traffic streams has a phase delay", see for example paragraph 4 of the Action of December 16, 2004.

The other cited reference, Pawelski, also does not teach the use of a buffers size or length to determine phase delay. Pawelski only describes adjusting an output signal to match the transmission rate of one of a number of reference phase signals by way of a phase alignment circuit (see for example, figure 4 and column 3, lines 42 to 54), and does not even discuss the use of buffers. Thus, neither Hiltner nor Pawelski describes or suggests the claimed features of claims 19 and 47, and as therefore, such claims are patentable over the cited prior art.

Further, claim 25 defines a delay that correlates to a length of a logical buffer and its associated transmission rate, and claim 40 provides that the length of a logical buffer, and other

things, are selected to achieve a relative delay. These claims were also rejected on the basis of figure 4 of Hiltner. However, as noted above, these features are not disclosed or suggested by Hiltner or Pawelski. For the same reasons already discussed, Applicant respectfully submits that claims 25 and 40 are also patentable in view of the prior art.

* * * * *

By way of the present response, this application is believed to be in condition for allowance and such action in due course is earnestly solicited. The Examiner is invited to contact the undersigned by telephone to discuss this case further, if necessary. Should further examination be necessary, in view of an absence of sufficient information regarding Hiltner in the last Office Action as noted above, Applicant requests that a specific identification of the features of the claims in the cited prior art be provided in a non-final action.

Respectfully submitted,

April 18, 2005
Date

Robert H. Nakano
(Registration No. 46,498)

McCarthy Tétrault LLP
Box 48, Toronto Dominion Bank Tower
Suite 4700, 66 Wellington Street West
Toronto, Ontario M5K 1E6 Canada